sent via the microwave link to DSS 13. The 30-MHz IF amplifier chain at DSS 13 had an adjustable delay line inserted in it. The delay line had a total delay of 126 μs adjustable in 2-μs steps from zero to maximum delay.

The final IF amplifier output at DSS 13, 455 kHz with a noise bandwidth of approximately 330 kHz, was correlated in real time with the 455-kHz signal from DSS 14 in an analog correlator. The analog output of the correlator was then recorded on another channel of the previously mentioned digital recorder. Also recorded on the remaining two channels of the digital recorder were the total power levels of the DSS 14 and DSS 13 receivers. This information may be used to obtain solar scintillation data.

The station provided the experiments with a total of seven observing periods; the first two on September 25 and 26, 1969, from 2100 to 0300 UT, and the one on October 1, 1969, from 0400 to 0900 UT, were used to check system operation. During the September 25 and 26 run, the *Mariner VI* spacecraft was tracked and fringes were observed from the *Mariner* spacecraft carrier. For this test, both stations operated at approximately 2297 MHz. The October 1 run utilized various radio sources and fringes were successfully observed on all sources tracked.

The actual experimental observations of 6 h each took place on October 2 and 3, October 4 and 5, October 6 and 7, October 10 and 11, and October 14 and 15, 1969, from approximately 2000 to 0200 UT.

The data from the general relativity experiment are being processed and evaluated by the experimenters.

B. DSIF Operations

1. RF Spectrum Analysis Technique Utilized by JPL Compatibility Test Area and Cape Kennedy Compatibility Test Station, *A. I. Bryan*

a. Introduction. One of the requirements of telecommunications compatibility testing of the spacecraft with the tracking and data system is to search the RF spectrum for extraneous, as well as expected, frequencies which are of sufficient amplitude to enable the S-band receiver to obtain phase lock.

The technique previously used to search for these RF signals required the receiver operator to manually tune the receiver and attempt to phase-lock the receiver. The receiver operator had to be able to hear a difference frequency as the receiver passed through a signal in the spectrum, and as a result, data on low-level signals were questionable. Consequently, in December 1967, a system was implemented at DSS 71 utilizing the digital instrumentation system (DIS) phase I digital computer (SDS-920) to provide: (1) S-band receiver voltage-controlled oscillator (VCO) tuning control, (2) frequency monitoring and frequency band power level measurements, and (3) RF spectrum data recorded on the line printer.

b. System configuration and description. A block diagram of the system is shown in Fig. 2. The S-band receiver heterodynes the incoming signal to produce a 10-MHz IF carrier, which is passed through a telemetry bandpass filter and is then mixed with 10.02-MHz to produce a 20-kHz carrier with telemetry subcarriers. The 20-kHz receiver output is input to a wave analyzer, which operates in the normal mode (no automatic frequency control) with a 6-Hz or 200-Hz bandpass.

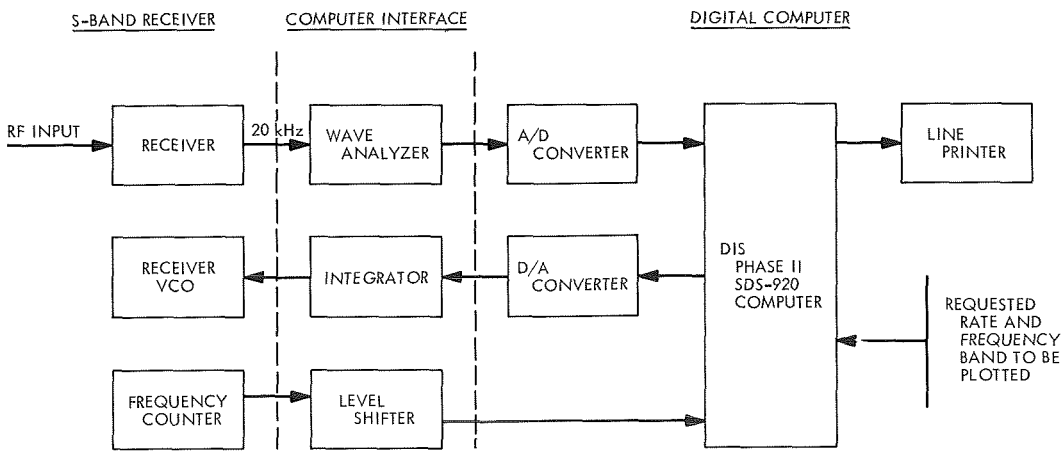

Fig. 2. Block diagram—RF spectrum analysis system

There are two time-multiplexed modes of operation of the system. The specific mode of the system is controlled by interrupts.

The mode with the lowest priority (mode I) is the servo-loop for frequency rate control. This mode provides closed-loop control of the receiver VCO. The digital computer functions as a digital comparator to form the difference between a requested frequency rate and the actual rate of frequency change. The computer then multiplies this difference error by a simple transfer equation. The resulting voltage from the digital-to-analog (D/A) converter drives a lowpass RC filter which provides the control voltage for the VCO. The bandwidth of the integrator is much smaller than that of the VCO, and consequently, the VCO tracks the integrator without significant delay. The RC filter acts to smooth and divide the step signal from the D/A converter.

The VCO frequency is monitored by the counter, which operates in a 1-s interval counter mode. The counter output closes the loop through the digital inputs of the computer. Constants, such as the desired frequency band to be analyzed, starting frequency, and the desired rate of change of frequency, are input to the computer from the typewriter console.

The mode with the highest priority (mode II) is concerned with the computation of the spectrum power. A 14-bit A/D converter samples the wave analyzer output. The computer then sums this information and correlates the sum data with the frequency-band information obtained from the frequency counters. Sampling of the data is sufficiently fast so the Nyquist frequency is not approached.

Mode III includes the output to the DIS line printer and consists of points which are plotted and tagged as to frequency and relative power to carrier level. The plot output is in decibels.

c. System analysis.

Mode I. The block diagram of Fig. 2 can be divided into a discrete and a continuous section, as illustrated in Fig. 3. The discrete section consists of the digital computer and sampler. The continuous section consists of the D/A converter and the integrator. The VCO and the computation time delay within the computer can be ignored due to their relatively high-frequency response in comparison to the desired system frequency response.

This discrete-data control system must be physically realizable with finite settling time and zero steady-state error for an input which is a constant. The condition of a specific input (step function) implies that a "minimal" response design is satisfactory.

Therefore, the closed-loop transfer function of the system (ignoring τ) in Fig. 3 is

$$M(Z) = \frac{C(Z)}{R(Z)} = \frac{D(Z)\,Gp(Z)}{1 + D(Z)\,Gp(Z)}$$

where

$$Gp(Z) = Z[G(S)] \qquad (1)$$

$$Z[G(S)] = Z\left[\frac{1 - e^{-TS}}{S}\,\frac{K_1}{S}\right] = \frac{K_1 T}{Z - 1}$$

where T is the sampling period of 1 s.

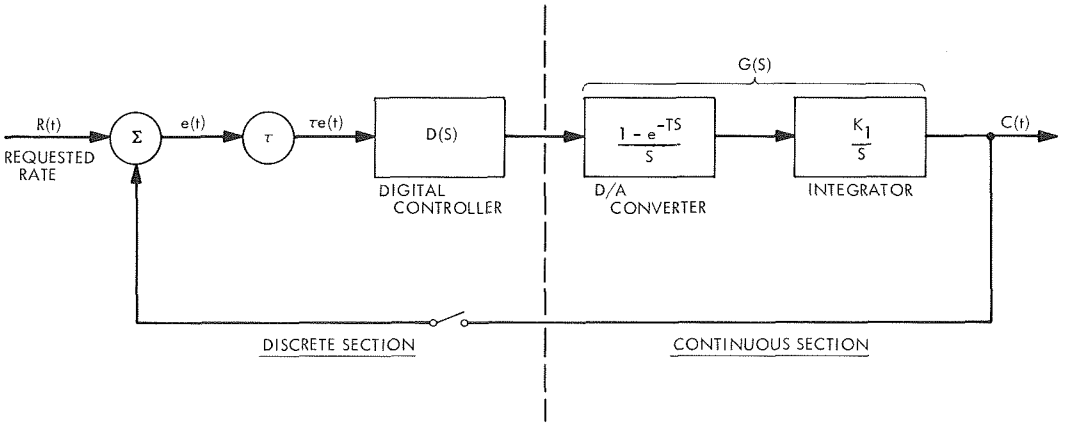

Fig. 3. Simplified block diagram—RF spectrum analysis system

Since the process $Gp(Z)$ has no time lag or zeroes (with the simplifying assumptions), then $M(Z)$, the system transfer function, is optimized for a step input by setting $M(Z) = Z^{-1}$ (Ref. 1).

Solving for $D(Z)$ in Eq. (1) yields

$$D(Z) = \frac{M(Z)}{1 - M(Z)} \times \frac{1}{Gp(Z)}$$

and substituting values yields

$$D(Z) = \frac{Z^{-1}}{1 - Z^{-1}} \times \frac{Z - 1}{K_1}$$

$$= \text{constant}\left(\frac{1}{K_1}\right)$$

where $K_1 = 0.0016$. If $D(Z)$ is selected for this value, then the output response is

$$C(Z) = \frac{1}{Z - 1} = Z^{-1} + Z^{-2} + Z^{-3} \cdots$$

The equation for $C(Z)$ implies that the system output will respond to the step input with a delay of one period of the sampling rate.

However, the ± 1 count in the counter does effect the loop; therefore, a variable dampening factor is utilized in the system. The factor $\tau = 1$ when driving the system toward a desired frequency position. The factor $\tau = 0.1$ is then selected by the program when rate and frequency position have been achieved. The value for $\tau = 0.1$ was selected by a system simulation on the SDS 920 and has the effect that $C(Z)$ does not reach zero steady-state for a step input until a delay of 7 sample periods.

The desired S-band frequency rates can be achieved from approximately 2 to 400 Hz/s.

Mode II. The wave analyzer (HP-302 or HP-310A) noise level and the S-band carrier are measured by the computer program and stored as constants. The frequency relationships to these data points and to the data points of the swept spectrum are obtained from the counters.

The voltage signal from the wave analyzer represents the signal power within the selected noise bandwidth of the analyzer. The sampled output of a particular spectrum interval (i.e., 5 Hz, if a 5-Hz/s rate is selected) is summed, squared, and expressed in volts. Then a comparison is made with the previously measured carrier power to form a relative level expressed in dB.

A machine language subroutine (SDS-920 symbolic) is required to speed the operation of handling the sampled data. The sample rate is a constant 333 samples/s. A 1-ms pulse from the station timing system is used to initiate the sample interrupt.

The graphic display of the RF spectrum allows real-time observation, as well as a permanent record of power and frequency measurements. Any portions of the spectrum may be further examined by plotting an expanded section (i.e., sweeping the spectrum at a slow rate) of the area in question. Results have shown that at power levels of -40 dB below the carrier, relative accuracies of ± 1 dB are obtained. An example of the output is illustrated in Fig. 4.

d. Development. To reduce the time involved in analyzing the spectrum, it is proposed to use the fast discrete Fourier transform (DFT) to examine the S-band spectrum. Preliminary testing has been successful in utilizing the Welch (SPS 37-40, Vol. III, pp. 6–8) version of the DFT to examine the spectrum from the carrier to approximately 160 kHz. The data obtained are comparable to the analog technique presently used. The time involved in a spectrum observation is reduced by a factor of 10 to 20.

Reference

1. Kuo, D. C., *Analysis and Synthesis of Sampled-Data Control Systems.* Prentice-Hall, Inc., Englewood Cliffs, N. J., 1963.

C. Facility Engineering

1. SFOF Emergency Power Subsystem, *R. V. Phillips*

a. Introduction. The SFOF emergency power subsystem discussed in SPS 37-50, Vol. II, pp. 189–191, SPS 37-51, Vol. II, pp. 170–171, and SPS 37-57, Vol. II, pp. 170–173, is incrementally becoming a reality. The uninterruptable power system (UPS) began on-line operation on May 3, 1969, and the engine-driven standby power plant is scheduled for completion in early 1970. The installation of the central supervisory monitor and control system is in process and will be operable with completion of the standby power plant.